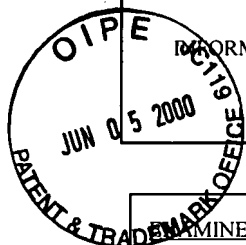


PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. P043D2C3C	SERIAL NUMBER 09/492,982
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE JANUARY 27, 2000	GROUP ART UNIT 2818



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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
TNT	4,330,852	May 18, 1982	Redwine et al.	365	221	
1	4,703,418	Oct. 27, 1987	James	364	200	
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TNT	S56-82961	July 7, 1981	Japan			YES
1	S57-14922	Jan. 26, 1982	Japan			YES
	Sho 60-80193	May 8, 1983	Japan			YES
	Sho 60-55459	Mar. 30, 1985	Japan			YES
	S61-72350	April 14, 1986	Japan			YES
	S63-142445	June 14, 1988	Japan			YES
	B63-46864	Sept. 19, 1988	Japan			YES
TNT	S64-29951	Jan. 31, 1989	Japan			YES

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TNT	Watanabe, T.; "Session XIX: High Density SRAMS"; IEEE International Solid State Circuits Conference pp. 266-267 (1987)
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EXAMINER <i>Tan T. Nguyen</i>	DATE CONSIDERED <i>07/31/00</i>
EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.	

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. P043D2C3C	SERIAL NUMBER 09/492,982
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TNT	0 246 767	April 28, 1987	EPO			
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EXAMINER <i>TAN T. NGUYEN</i>	DATE CONSIDERED <i>07/31/00</i>
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